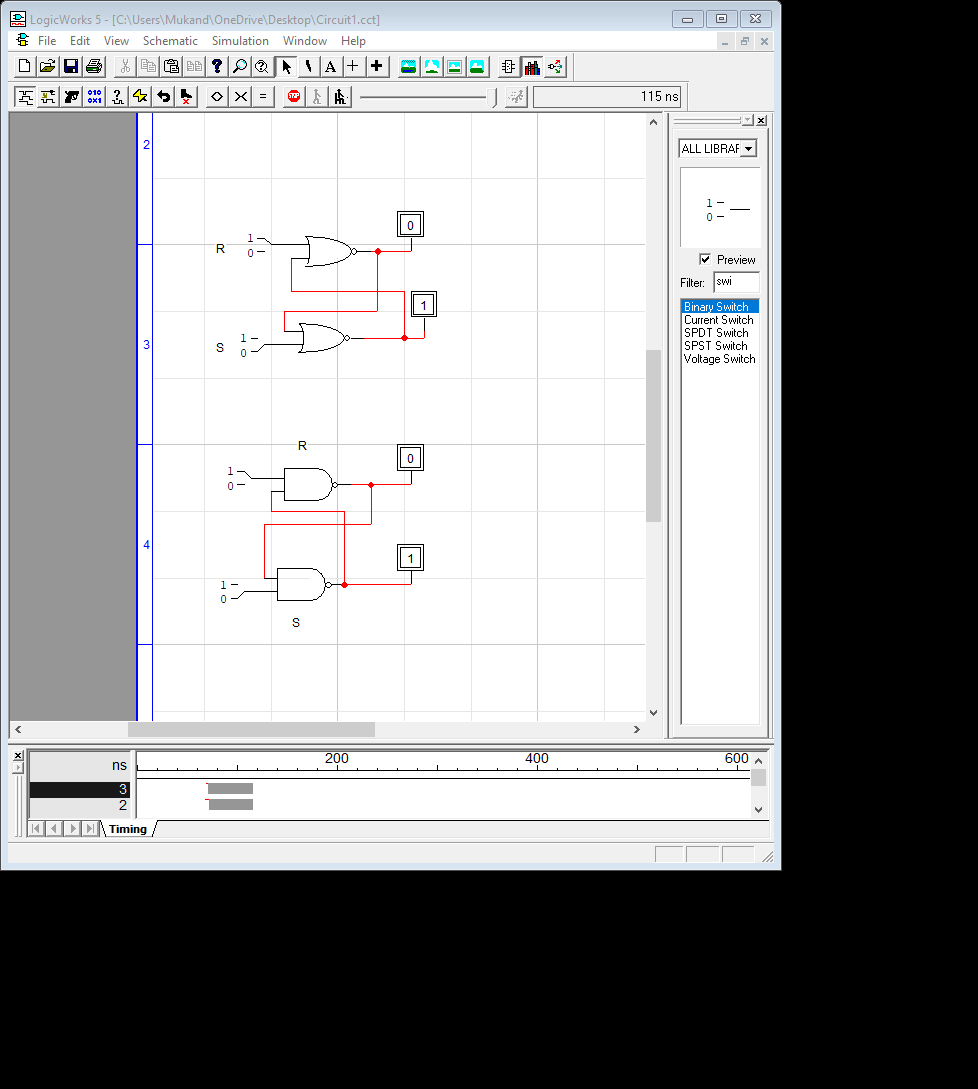
**LAB # 11 Assignment**

**Roll no: 20k-0409 Name: Mukand**

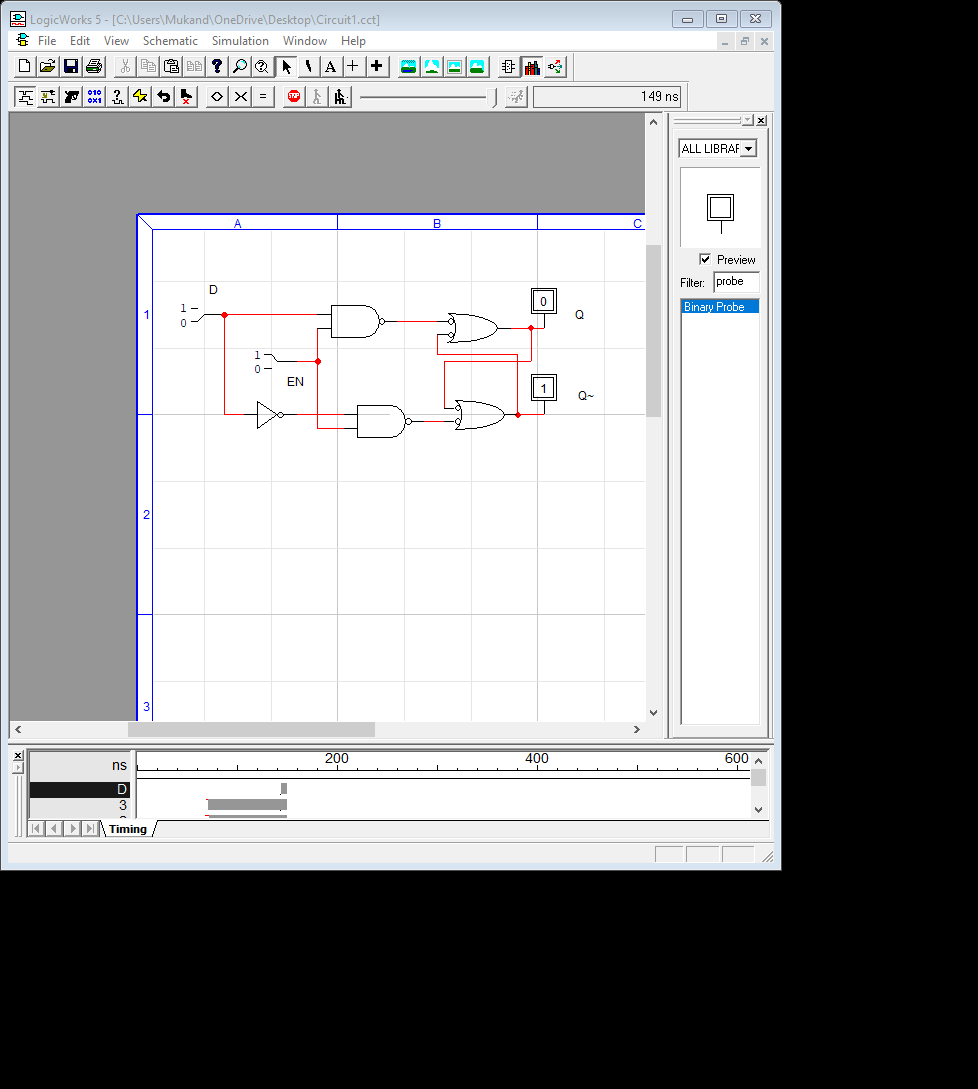
Ques 1:

**Implement SR Latch by using logic gates.**

 Nor and Nand gate

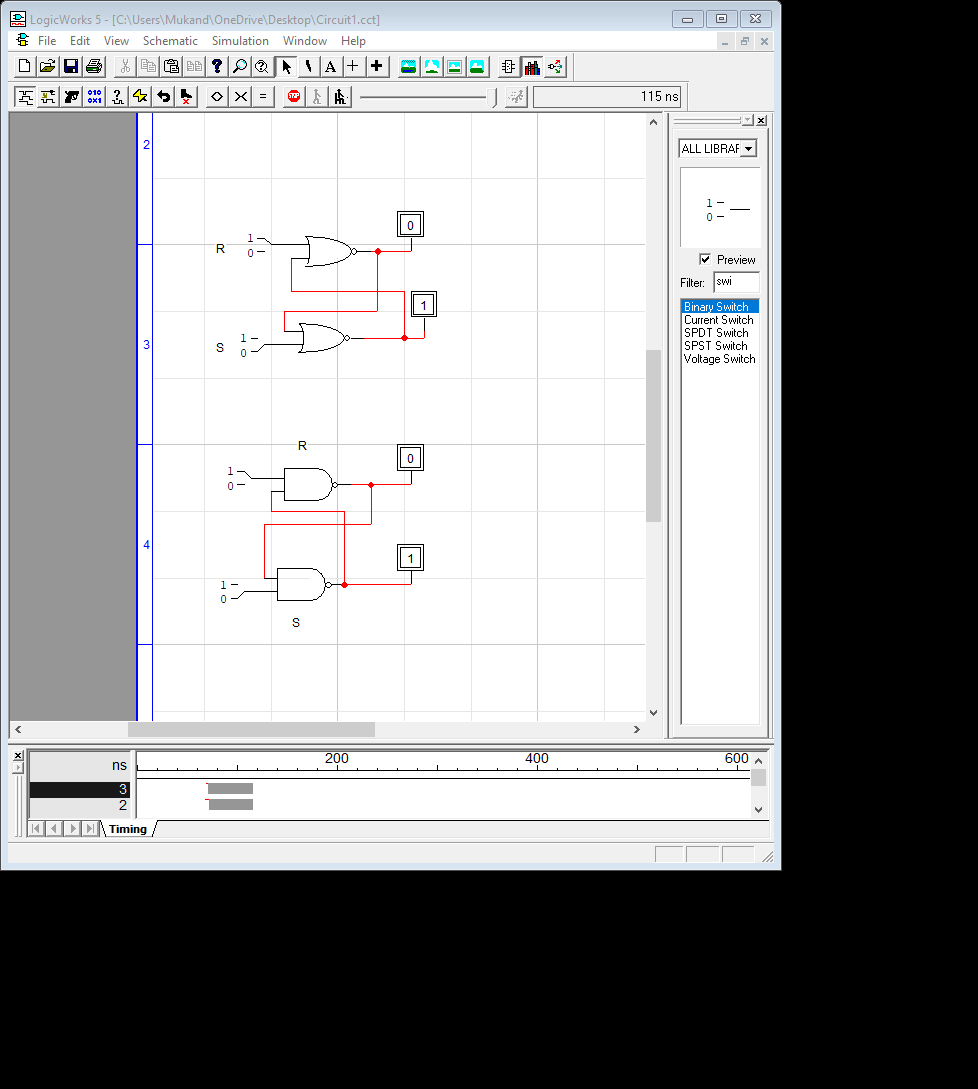
**Ques 2:**

**Implement D Latch by using logic gates.**



**Ques 3:**

Implement S-R latch using nand and nor gates



**Ques 4:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S | R | Qn | Q | Q~ |
| 0 | 0 | 0 | Memory | Memory |
| 0 | 0 | 1 | Memory | Memory |
| 0 | 1 | 0 | 0 (reset) | 1(reset) |
| 0 | 1 | 1 | invalid | Invalid |
| 1 | 0 | 0 | 1 (set) | 0 (set) |
| 1 | 0 | 1 | invalid | Invalid |
| 1 | 1 | 0 | invalid | invalid |
| 1 | 1 | 1 | Invalid | invalid |